Samskruti College of Engineering and Technology
Kondapur, Telangana 501301

(Affiliated to JNTUH, Hyderabad & Approved by AICTE, New Delhi)

MODEL LESSON PLAN
STLD

UNIT-I			
Lecture No	**Name of the topic**	**References**	**Teaching Method**
L1	Introduction,Review of number systems	**T1,R1**	Chalk/Talk
L2	Complements of Numbers	**T1,R1**	Chalk/Talk
L3	Codes- Binary Codes	**T1,R1**	Chalk/Talk
L4	Binary Coded Decimal Code	**T1,R1**	Chalk/Talk
L5	Codes and Properties	**T1,R1**	Chalk/Talk
L6	Unit Distance Codes	**T1,R1**	Chalk/Talk
L7	Error Detecting and Correcting Codes	**T1,R1**	Chalk/Talk
L8	Boolean Algebra Theorems and Properties	**T1,R1**	Chalk/Talk
L9	Switching Functions, Canonical and Standard Form	**T1,R1**	Chalk/Talk
L10	Digital Logic Gates, XOR Gates	**T1,R1**	Chalk/Talk
L11	Universal Gates	**T1,R1**	Chalk/Talk
L12	Multilevel NAND/NOR realizations	**T1,R1**	Chalk/Talk
UNIT-II			
L13	Introduction, The Minimization of switching function using theorem	**T1,R1**	Chalk/Talk
L14	The Karnaugh Map Method-Up to Five Variable Maps	**T1,R1**	Chalk/Talk
L15	Don't Care Map Entries	**T1,R1**	Chalk/Talk
L16	Tabular Method, Design of Combinational Logic	**T1,R1**	Chalk/Talk
L17	Adders, Subtractors, comparators	**T1,R1**	Chalk/Talk
L18	Multiplexers, Demultiplexers	**T1,R1**	Chalk/Talk
L19	Decoders, Encoders and Code converters, Hazards and Hazard Free Relations.	**T1,R1**	Chalk/Talk

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UNIT-III			
L24	Basic Architectural	**T1,R1**	Chalk/Talk
L25	Distinctions between Combinational and Sequential circuits, The Binary Cell,	**T1,R1**	Chalk/Talk
L26	Fundamentals of Sequential Machine Operation	**T1,R1**	Chalk/Talk
L27	Latches, Flip Flops: SR, JK, Race Around Condition in JK	**T1,R1**	Chalk/Talk
L28	JK Master Slave, D and T Type Flip Flops	**T1,R1**	Chalk/Talk
L29	Excitation Table of all Flip Flops, Design of a Clocked Flip-Flop	**T1,R1**	Chalk/Talk
L30	Timing and Triggering Consideration,	**T1,R1**	Chalk/Talk
L32	Clock Skew, Conversion from one type of Flip-Flop to another	**T1,R1**	Chalk/Talk
L33	Shift Registers, Data Transmission in Shift Registers	**T1,R1**	Chalk/Talk
1.34	Operation of Shift Registers, Shift Register Configuration	**T1,R1**	Chalk/Talk
1.35	Bidirectional Shift Registers, Applications of Shift Registers	**T1,R1**	Chalk/Talk
1.36	Design and Operation of Ring and Twisted Ring Counter	**T1,R1**	Chalk/Talk
1.36	Operation Of Asynchronous And Synchronous Counters	**T1,R1**	Chalk/Talk
UNIT-IV			
L37	Introduction, State Diagram, Analysis of Synchronous Sequential Circuits	**T1,R1**	Chalk/Talk
L38	Approaches to the Design of Synchronous Sequential Finite State Machines	**T1,R1**	Chalk/Talk
L39	Synthesis of Synchronous Sequential Circuits	**T1,R1**	Chalk/Talk

L40	Serial Binary Adder	**T1,R1**	Chalk/Talk
L41	Sequence Detector	**T1,R1**	Chalk/Talk
L42	Parity-bit Generator	**T1,R1**	Chalk/Talk
L43	Design of Asynchronous Counters	**T2,R1**	Chalk/Talk
L44	Design of Synchronous Modulo N – Counters	**T1,R1**	Chalk/Talk
UNIT-V			
L47	Finite state machine-capabilities and limitations	**T2,R1**	Chalk/Talk
L48	Mealy and Moore models-minimization of completely specified and incompletely specified sequential machines	**T1,R1**	Chalk/Talk
L49	Partition techniques	**T1,R1**	Chalk/Talk
L50	Merger chart methods-concept of minimal cover table	**T1,R1**	Chalk/Talk

TEXT BOOKS:

1. Switching and Finite Automata Theory- Zvi Kohavi & Niraj K. Jha, 3rdEdition, Cambridge.
2. Digital Design- Morris Mano, 5rd Edition, Pearson.

REFERENCES:

1. Modern Digital electronics RP Jain 4th Edition, McGraw Hill
2. Switching Theory and Logic Design – A Anand Kumar, 3rd Edition, PHI, 2013.